Amendment to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory arrangement comprising:

a programmable memory;

a first buffer memory associated with the programmable memory, to which first buffer memory, ~~in the case of~~ responsive to a request for a program command which is accessed in the programmable memory ~~access~~, a plurality of commands ~~at least one command~~ following the accessed command in the programmable memory are [[is]] written, wherein a first information line associated with the first buffer memory is used for command transfer, and wherein the accessed command and the plurality of commands ~~at least one command~~ following the accessed command are simultaneously stored in sequential memory locations of the first buffer memory; and

a second buffer memory to which, ~~in the case of~~ responsive to a request for a [[data]] datum which is accessed in the programmable memory ~~access~~, a plurality of data ~~at least one datum~~ following the accessed datum in the programmable memory are [[is]] written, wherein a second information line associated with the second buffer memory is used for data transfer, and wherein the accessed datum and the plurality of data ~~at least one datum~~ following the accessed datum are simultaneously stored in sequential memory locations of the second buffer memory;

wherein at least one of the first buffer memory and the second buffer memory is one of integrated in the programmable memory and connected to the programmable memory; [[and]]

wherein the respective ones of the plurality of commands ~~at least one command~~ following the accessed command are associated with respective ones of [[and]] the plurality of data ~~at least one datum~~ following the accessed datum ~~are associated with one another~~ by corresponding respective sequential positions of the respective ones of the plurality of commands ~~at least one command~~ within the first buffer memory and the respective ones of the plurality of data ~~at least one datum~~ within the second buffer memory; and

wherein, based on the association, each of the respective ones of the plurality of data is processed in accordance with the respective datum's associated command.

2. (Original) The memory arrangement according to claim 1, wherein the programmable memory includes a burst flash memory.

3. (Original) The memory arrangement according to claim 1, wherein the second buffer memory is loaded only in the case of a data access.

4. (Currently Amended) The memory arrangement according to claim 1, wherein content of the first buffer memory is not changed when the plurality of data ~~at least one datum~~ is subsequently read from the second buffer memory.

5. (Currently Amended) A buffering method for performance ~~performing at least one of a command access and a data access~~ during a program execution in connection with a programmable memory, comprising the steps of:

recognizing in the case of a request for a program command which is accessed in the programmable memory ~~access~~ that a command access is present;

recognizing in the case of a request for a datum which is accessed in the programmable memory ~~data access~~ that a data access is present;

responsive to the command request, writing a plurality of commands ~~command~~ following the accessed command in the programmable memory to a first buffer memory, wherein a first information line associated with the first buffer memory is used for command transfer, and wherein the accessed command and the plurality of commands ~~command~~ following the accessed command are simultaneously stored in sequential memory locations of the first buffer memory; and

responsive to the datum request, writing a plurality of data [[datum]] following the accessed datum in the programmable memory to a second buffer memory, wherein a second information line associated with the second buffer memory is used for data transfer, and wherein the accessed datum and the plurality of data [[datum]] following the accessed datum are simultaneously stored in sequential memory locations of the second buffer memory;

wherein at least one of the first buffer memory and the second buffer memory is one of integrated in the programmable memory and connected to the programmable memory; [[and]]

wherein ~~the command and~~ respective ones of the plurality of commands are associated with respective ones of the [[datum]] plurality of data ~~are associated with one another~~ by corresponding respective sequential positions of the respective ones of the plurality of commands ~~at least one command~~ within the first buffer memory and the

respective ones of the plurality of data ~~at least one datum~~ within the second buffer memory; and

wherein, based on the association, each of the respective ones of the plurality of data is processed in accordance with the respective datum's associated command.

6. (Original) The method according to claim 5, further comprising the step of:

shifting access to the programmable memory between the first buffer memory and the second buffer memory as a function of whether the command access or the data access is desired.

7. (Original) The method according to claim 6, wherein the step of shifting access is determined by an address matcher that recognizes whether the command access or the data access is desired.

8. (Original) The method according to claim 6, wherein the step of shifting access is determined by at least one signal of a processor which indicates whether the command access or the data access is desired.